PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	Docket No: Q88131
Hitoshi YANO, et al.	Group Art Unit: 2817
Appln. No.: 10/537,470	Examiner: Hieu P. NGUYEN
Confirmation No.: 3255	Patent No.: 7,298,215
Filed: June 3, 2005	Issue Date: November 20, 2007

For: AMPLIFYING CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to the provisions of 37 C.F.R. § 1.322, please enter the attached Certificate of Correction.

Since the errors noted are believed to be the fault of the Patent and Trademark Office, we are not enclosing the $100.00 Certificate of Correction fee. If it is found to be to the contrary, please charge our Deposit Account No. 19-4880.

In view of the foregoing, issuance of the Certificate of Correction is respectfully requested.

Respectfully submitted,

Carl J. Pellegrini
Registration No. 40,766

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WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: August 12, 2008

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO: 7,298,215

DATED: November 20, 2007

INVENTOR(S): Hitoshi YANO

Tomoyuki YAMASE

Keiichi NUMATA

Tadashi MAEDA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 1, Line 18, delete "**PRIOR**" insert --**DESCRIPTION OF THE RELATED ART**--

Col. 1, Line 48, after "**seleted**" insert--.--

Col. 1, Line 67, delete "**index**" insert --**figure**--

Col. 2, Line 36, before the paragraph begining with " **In view of the above etc**." insert the Title --**SUMMARY OF THE INVENTION**--

Col. 2, Line 49, after "In", delete "**order to accomplish the above mentioned object**" insert --**one aspect**--

Col. 3, Line 44, before "**The present invention**", insert --**In another aspect**--

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INVENTOR(S): Hitoshi YANO

Tomoyuki YAMASE

Keiichi NUMATA

Tadashi MAEDA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 3, Line 54, after paragraph ending with "**impedance**" and before the title "**BRIEF DESCRIPTION OF DRAWINGS**",
insert--The advantages obtained by the aforementioned present invention will be described hereinbelow.

In accordance with the present invention, the control circuit makes input and/or output impedances high. Hence, it would be possible to switch electrical connection to disconnection and vice versa without arranging a switch into a signal path. Furthermore, it would be possible to accomplish a high gain in low power consumption without a loss caused by arranging a switch into a signal path.

In addition, since it is possible to cancel reduction in an impedance in a high-frequency band, caused by a parasitic capacity in an amplifying device, with an inductance device, it would be possible to accomplish a high impedance in a high-frequency band. Furthermore, since it is possible to cancel reduction in an impedance with an inductance device which resonate in parallel with a parasitic capacity at a certain frequency, it would be possible to accomplish a high impedance at the certain frequency.

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The gain-variable amplifying circuit in accordance with the present invention makes input/output impedance high, when an amplifying circuit(s) constituting the gain-variable amplifying circuit is(are) not selected. Hence, it is possible to maintain a high gain, regardless of a number of amplifying circuits electrically connected in parallel with one another, ensuring that there are accomplished a high gain, a low noise figure, and low current consumption, even in a broad band in which a gain varies, or even at a narrow step by which a gain varies

The above and other objects and advantageous features of the present invention will be made apparent from the following description made with reference to the accompanying drawings, in which like reference characters designate the same or similar parts throughout the drawings.--

Col. 4, Line 10, Line 14, Line 18, Line 21 delete "**a**" and "**b**" insert --**A**-- and --**B**--

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 4, Line 31, through Col. 5 Line 3 delete entire paragraph titled **--Indication by Reference Numerals--**

Col. 5, Line 5, delete **--DETAILED--**

Col. 7, Lines 1, 5, 8, 10, 14, 17, 18 delete "**a**" and "**b**" and insert **--A--** and **--B--**

Col. 11, Lines 52, 54, 57 delete "**a**" and "**b**" insert **--A--** and **--B--**

Col. 12 Lines 9, 10, 21, 27, 36, 38, 40, 44, 45, 47, 49, 52, 56, 58, 61, 62, and 63 delete "**a**" and "**b**" insert **--A--** and **--B--**

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 13, Line 1, insert paragraph beginning with

--While the present invention has been described in connection with certain preferred embodiments, it is to be understood that the subject matter encompassed by way of the present invention is not to be limited to those specific embodiments. On the contrary, it is intended for the subject matter of the invention to include all alternatives, modifications and equivalents as can be included within the spirit and scope of the following claims.

The entire disclosure of Japanese Patent Application No. 2002-352664 filed on December 4, 2002 including specification, claims, drawings and summary is incorporated herein by reference in its entirety.--

Col. 13, Lines 1-29, delete paragraph titled **--INDUSTRIAL APPLICABILITY--**

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 2, Line 36, at the end of paragraph titled "**Description of the Related Art**" insert --Japanese Patent Application Publication No. 5-206818 has suggested a semiconductor switch comprised of (a) a first hybrid circuit, (b) first and second circuits each having an input end electrically connected to a pair of input/output terminals of the first hybrid circuit, and (c) a second hybrid circuit having a pair of input/output terminals each electrically connected to an output end of the first circuit and an output end of the second circuit. The first and second circuits include bias means comprised of a field effect transistor and an inductor for applying a bias voltage to a gate electrode of the field effect transistor. The first and second circuits define a filter which allows a certain frequency to pass therethrough in a bias condition where a high impedance is defined across drain and source electrodes of the field effect transistor.

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Keiichi NUMATA

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Japanese Patent Application Publication No. 2000-332545 has suggested a low-noise amplifying circuit including an input matching circuit, a low-noise amplifier, and an output matching circuit, and a switch accomplishing electrical connection between input and output of said low-noise amplifier, and a compensation circuit electrically connected to the switch for compensating for an impedance. The switch is comprised of two switches electrically connected in series between input and output of the low-noise amplifier. The compensation circuit is arranged between a node at which the two switches are electrically connected to each other, and a grounded voltage.

Japanese Patent Application Publication No. 2000-349574 has suggested a high-power amplifier including N high-frequency amplifiers, a bias controller for turning on or off each of the N high-frequency amplifiers, N input transmission lines arranged between input terminals of the N high-frequency amplifiers and a common input terminal, and N output transmission lines arranged between output terminals of the N high-frequency amplifiers and a common output terminal. By turning on or off the N high-frequency amplifiers, matching/mismatching is controlled between the N high-frequency amplifiers and the input transmission lines to thereby control an impedance observed when viewed from the common input terminal towards the input transmission lines, and an impedance observed when viewed from common output terminal towards the output transmission lines.

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Keiichi NUMATA

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Japanese Patent Application Publication No. 5-299995 has suggested a micro-wave semiconductor switch comprised of a first semiconductor switch and a second semiconductor switch. A first circuit is comprised of the first semiconductor switch and an inductance L electrically connected in series to each other. A second circuit is comprised of a second semiconductor switch including an inductor La arranged between terminals, and a capacitor C electrically connected in series with the inductor La. The first and second circuits are electrically connected in parallel with each other. The first and second semiconductor switches are designed to operate in such a manner that if one of the first and second semiconductor switches is on, the other is also on. An inductance of the inductor La and a capacity of the capacitor C are determined such that La (C + Cs) = LC wherein Cs indicates a parasitic capacity between terminals in each of the first and second semiconductor switches. The following equation is established at an operational frequency F.

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$F = 1/(2\pi\ (LC)^{1/2})$

Japanese Patent Application Publication No. 2000-307456 has suggested a tuner including a frequency-variable filter making synchronization with a frequency of a received high-frequency signal, a frequency-variable terminator arranged upstream of the frequency-variable filter and causing a small loss in a frequency band in which the frequency-variable filter allows a signal to pass therethrough, and a certain impedance in a reflection band of the frequency-variable filter, and a frequency converter which combines a high-frequency signal having passed through the frequency-variable filter, with a local oscillation signal associated with the high-frequency signal, to thereby produce an intermediate-frequency signal.--.

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